A Practical Methodology for Calculating Acceptable IR Drop Targets in Advanced VDSM Design

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Introduction
Smaller process geometries have led to a dramatic increase in problems due to “IR drop”—i.e., the voltage drop across a chip’s power network. As the term implies, IR drop results from the current and resistance associated with the power network.

Many papers on IR drop have focused on early “order-of-magnitude” calculations [1, 2] or complete analysis solutions for large and complex SoCs [3]. Such papers describe the analysis and design of power networks with the assumption that the networks are measured against a predetermined target for IR drop.

Rather than replicate the analysis and mitigation techniques described in these papers, the goal in this paper is to determine what an acceptable IR drop target should be. Indeed, this paper may be considered as a prequel to the earlier IR drop papers (see References) to form a complete chain of reference material for quantitative decision making in SoC design. Of course, much of the value in setting a target depends on when the target is set in the design process. Since much of the data described in the proposed methodology becomes available at different times for different projects, this paper cannot prescribe exactly when the target should be set. However, the earlier that the target can be provided as a specification to the physical implementation team, the better they will be able to design a robust power distribution network. As in most design specifications, as tradeoffs are examined by the implementation team, the final target will often be determined in an iterative fashion.

The problems caused by IR drop
Why worry about IR drop? The answer lies in two distinct problem areas.

First, the primary concern is that a reduced voltage difference between the V_{DD} and V_{SS} pins of a standard cell will reduce the cell’s operating performance. If the cell is on a critical path, the decrease in cell performance could reduce the chip’s operating frequency. The IR drop also reduces the cell’s noise immunity and in extreme cases can lead to functional failures.

It is vitally important to predict such real-world problems with static timing analysis (STA) tools such as Synopsys’ Primetime® SI. Leading STA tools have the ability to predict the operational performance of a standard cell based on a case-by-case voltage level applied to the cell. However, most of the STA signoff process still assumes that all standard cells have the same max (V_{DD} plus 10 percent minus 0V), nom (V_{DD} minus 0V), and min (V_{DD} minus 10 percent minus 0V) applied to them. Note that these calculations assume that V_{DD} varies by ±10 percent, but V_{SS} is assumed to stay at 0V.

The second IR drop problem area involves library characterization. The standard cells in a library are characterized to give accurate predictions of their real-world performance over specified ranges of voltage, temperature and silicon processing conditions. As process geometries have shrunk, the equations needed to keep the predicted performance correlated to the measured silicon have become more complex, and significant deviations now occur when a standard cell operates outside of its characterized range.

Therefore, when performing STA on a design using “min” conditions, it is important to ensure that the minimum voltage seen by a standard cell is within the library’s characterization conditions. Otherwise, STA cannot accurately predict the real-world silicon performance.

Sources of IR drop
As mentioned earlier, a major cause of IR drop is the resistance of the power network combined with that network’s ability to source and sink current from the VDD and VSS pins. There are other potential causes of a loss of voltage to the SoC’s standard cells, however, and those causes involve the system in which the SoC operates.

Typically, an SoC is placed on a PCB and interfaces with other devices on the PCB. The system’s power supply is also on the PCB or nearby. A typical voltage regulator [4] provides a voltage that is stable within 1.5 to 2 percent of its target output. The power supply voltage is delivered to the SoC via the PCB’s power
distribution network. It has been estimated [5] that today’s high-speed, multilayer PCBs can show up to 18.5 mV of voltage drop from the voltage regulator to the furthest devices on the PCB, although a value between 11 and 14 mV is typical.

Thus, the total IR drop can be given as:

\[ IR_{\text{total}} = IR_{\text{pcb}} + IR_{\text{chip}} \]  

(1)

where \( IR_{\text{pcb}} \) consists of IR drop associated with supplying the SoC with power, and \( IR_{\text{chip}} \) consists of the IR drop on the SoC itself.

**Calculation of Acceptable IR drop targets**

To demonstrate a practical method for determining an acceptable IR drop targets, the following calculation uses the example of a typical 130 nm SoC and a 1.2V power supply. The starting assumptions are thus:

- A standard cell library characterized to 1.2V +/- 10 percent
- A power supply on the PCB of 1.2V +/- 2 percent
- 18.5 mV of IR drop from the power supply to the SoC

Based on the standard cell characterization data, it is clear that the SoC power network must maintain at least 1.08V (1.2V minus 10 percent) to all the standard cells. Also clear from the starting assumptions is that the worst-case voltage delivered from the power supply is 1.176V (1.2V minus 2 percent). A target IR drop is easily determined by subtracting the voltage requirement from the voltage supplied:

\[ IR_{\text{target}} = V_{\text{supply}} - V_{\text{require}} \]

\[ = 1.176V - 1.08V \]

\[ = 0.096V \text{ (96 mV)} \]

Letting \( IR_{\text{target}} \) be \( IR_{\text{total}} \) in equation (1) and using the 18.5 mV IR drop assumed on the PCB gives a new target for the IR drop on the SoC:

\[ IR_{\text{chip}} = IR_{\text{target}} - IR_{\text{pcb}} \]  

(2)

\[ = 96 \text{ mV} - 18.5 \text{ mV} \]

\[ = 77.5 \text{ mV} \]

Assuming an even split between \( V_{\text{DD}} \) fall and \( V_{\text{SS}} \) rise, an initial target for the power network design might be 38.75 mV on each of the \( V_{\text{DD}} \) and \( V_{\text{SS}} \) networks from the pins of the SoC to the standard cells. However, this target still presents a somewhat vague and potentially misleading requirement to the physical designer because the specified drop must be shared between the SoC’s package and die. The target needs to be further defined by considering:

\[ IR_{\text{chip}} = IR_{\text{package}} + IR_{\text{die}} \]  

(3)

where \( IR_{\text{package}} \) consists of IR drop within the package, and \( IR_{\text{die}} \) consists of IR drop on the die. The latter component can be further broken down as:

\[ IR_{\text{die}} = IR_{\text{pads}} + IR_{\text{core}} \]  

(4)

where \( IR_{\text{pads}} \) consists of IR drop across the bond pads and the I/O cell, and \( IR_{\text{core}} \) consists of IR drop from the I/O cell to the furthest standard cell. Note that the location of the “furthest” standard cell depends on both floorplan considerations and circuit operation. Figure 1 shows the individual components of \( IR_{\text{chip}} \) leading to \( IR_{\text{core}} \).
Combining (3), (4), and the value for $\text{IR}_{\text{chip}}$ found in (2), provides a formula for determining an actionable IR drop target for the physical design process:

$$\text{IR}_{\text{core}} = 77.5 \text{ mV} - \text{IR}_{\text{package}} - \text{IR}_{\text{pads}}$$  (5)

To determine values for $\text{IR}_{\text{package}}$ and $\text{IR}_{\text{pads}}$, consider that $\text{IR}_{\text{package}}$ consists of two components:

$$\text{IR}_{\text{package}} = \text{IR}_{\text{trace}} + \text{IR}_{\text{bondwire}}$$

where $\text{IR}_{\text{trace}}$ is IR drop across the traces in the package, and $\text{IR}_{\text{bondwire}}$ is IR drop across the bond wire. Values for these parameters vary greatly depending on package type, the number of package pins dedicated to $V_{\text{DD}}$ and $V_{\text{SS}}$, and the total power dissipation of the device; therefore, calculating these values is beyond the scope of this paper. Package vendors should be consulted when performing these calculations for an SoC project. For illustrative purposes, the calculations that follow assume 10 mV for $\text{IR}_{\text{package}}$.

The design team can calculate $\text{IR}_{\text{pads}}$ based on the resistance of the wires in the I/O cell, as provided by the I/O cell vendor or extracted during the design process. This resistance is multiplied by the current that the cell is expected to carry. Two alternatives for this current are possible:

- Absolute worst case based on the cell design and current-carrying limits inherent to the technology
- Expected worst case based on the expected power dissipation of the SoC and the number of $V_{\text{DD}}$ (or $V_{\text{SS}}$) cells in the SoC

The choice depends on the desired margin and the accuracy of the expected power dissipation of the SoC. Again, the following calculations assume 10 mV for $\text{IR}_{\text{pads}}$.

Substituting the calculated and assumed values into (5) gives:

$$\text{IR}_{\text{core}} = 77.5 \text{ mV} - 10 \text{ mV} - 10 \text{ mV}$$

$$= 57.5 \text{ mV}$$

This value has to be split between the allowable $V_{\text{DD}}$ fall and $V_{\text{SS}}$ rise. Dividing the value evenly gives a target IR drop of 28.75 mV for each network from the I/O cell to the furthest standard cell. The split does not have to be perfectly even, of course, so long as the total drop between the two supply rails does not exceed the target.

Appendix 1 shows similar calculations for typical voltages found in 180 and 90 nm process technologies. Appendix 2 shows how the calculations change when using a flip-chip design approach.
Conclusions
This paper has defined the scope of IR drop in an SoC as the network from the voltage regulator to the standard cells, and it has provided a methodology to calculate an acceptable IR drop budget for the SoC. The example calculation shown here for a typical SoC can serve as a starting point for design-specific calculations.

A similar methodology can be used for SoCs that have multiple voltage domains. Simply apply the calculations to each voltage domain independently.

References

Appendix 1 – Target IR Drop Calculations for Different Process Technologies
Table 1 shows the results of IR drop calculations for different process technologies. These calculations are based on the same types of assumptions described in the body of this paper. Consistent with the description in Section 4, units for the voltage parameters (\(V_{\text{nominal}}\), etc.) are volts, and units for the IR drop parameters are millivolts.

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<td>(IR_{\text{core}(VSS)})</td>
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Table 1. Calculated IR drop target values for 180, 130 and 90 nm
Appendix 2—Target IR Drop Calculations for Flip-Chip Designs

The calculated IR drop results shown in Table 2 are for a flip-chip design approach rather than the wire-bond approach assumed for the other calculations in this paper. The main differences are in assumptions for the calculations of IR\textsubscript{package} and IR\textsubscript{pads}. Because flip-chip designs have no bond wires, IR\textsubscript{package} is simply the IR drop in the package lead frame. In the case of IR\textsubscript{pads}, flip-chip designs typically have an array of V\textsubscript{DD} and V\textsubscript{SS} bump locations across the core area of the die, so very little IR drop occurs in the pad cell. As described in Section 4, many variables associated with the calculation of these parameters depend on the particular details of each chip. For illustrative purposes, Table 2 assumes IR\textsubscript{package} and IR\textsubscript{pads} values of 3 and 1 mV, respectively. Consistent with the description in Section 4, units for the voltage parameters (V\textsubscript{nominal}, etc.) are volts, and units for the IR drop parameters are millivolts.

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Table 2. Calculated Flip-Chip IR Drop Target Values

Comparing the last two rows in Tables 1 and 2 reveals one of the benefits of moving to a flip-chip design approach: the allowable IR drop budget increases. Additionally, the flip-chip design’s power grid is generally easier to design because the distance from the VDD and VSS bumps to the “furthest standard cell” is typically less than the corresponding distance in a wire-bond device. Both of these flip-chip advantages come at the expense of a higher-cost packaging solution, so the full set of tradeoffs must be examined.
Author Biography

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Michael has over 20 years of experience in the semiconductor industry. He has worked in engineering, marketing, and management roles at Motorola, Advanced Micro Devices, Ross Technology, and was president of The Silicon Group, a design services company in Austin, Texas. He graduated from The University of Texas with a bachelor's degree in electrical engineering and from The Wharton School with a master's degree in business administration.

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Jonathan is responsible for physical-design projects in Europe and Asia. With over 15 years experience in the semiconductor industry he has held engineering and management positions at Texas Instruments and Sony prior to joining Synopsys. He holds a bachelor's degree with honors in electrical and electronic engineering from the University of Reading, UK.